Hardware and software aspects of screen handling on the VZ-200/300 Part 1

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This article describes the hardware aspects of the Motorola MC6847 Video Display Generator chip which is used in a number of microcomputers. Although this is an older device and lacks some of the features of newer chips, it is nevertheless a well-used device and is quite easy to interface and comprehend. To illustrate the MC6847, its use in the VZ-200 and VZ-300 computers is detailed. Additionally, some software implementations are explained and some simple hardware modifications to the VZ are given to improve screen resolution and display appearance.

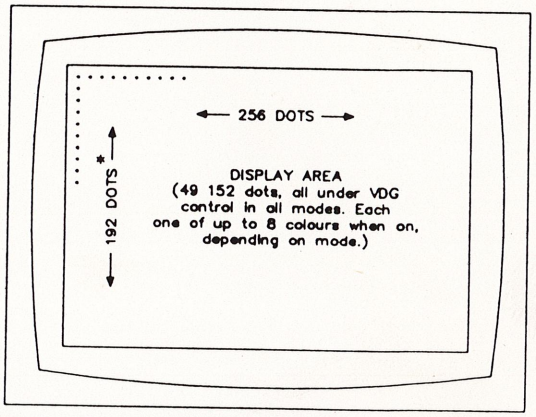
THE MOTOROLA MC6847 Video Display Generator (VDG) chip (sometimes referred to as a Cathode Ray Tube Controller — CRTC) is used to interface data read from the video RAM section of memory and to produce a modulated RF video signal or monitor output. The MC6847 is capable of operating in 14 different display modes. However, only a few of these are usually implemented in a particular installation. The MC6847 was conceived as one of the family of devices to interface with the Motorola M6800 and M68000 microprocessor families, but it can easily be adapted to other microprocessors. The VDG can be found in video games, home computers, process control displays, communications and graphics applications.

The VDG has the complex task of converting data from the screen memory into the form necessary for the raster scan display used in television and monitors. On these devices, the image is 'drawn' on the screen one horizontal scan line at a time. The 'spot' moves across the screen from right to left and its brightness or colour (chroma) is varied to produce the required display. In practice, the whole screen is built up in two passes, the first on even-numbered lines and the second on odd-numbered lines, by a process called 'interlacing' which helps to avoid flicker. The process occurs every 20 ms, or 50 half-frames are drawn every second.

Two types of VDG chip are produced by Motorola — the MC6847 for non-interlaced displays and the MC6847Y which interlaces the video display. the suffix 'P' after the device number identifies a plastic package. An enhanced version — the MC6847T1 — is also available but it is not strictly compatible with the MC6847 as it requires less external circuitry and has some additional features.

A timing or clock pulse is required to tie the scan rate and memory access cycles of the VDG in with that of the microprocessor (MPU) — otherwise chaos would reign on the bus systems! An external (to the VDG) clock is used to synchronise both the VDG and the MPU. A clock frequency of 3.58 MHz is usually selected to give the correct scan rates. If a common clock is used then often the speed of the MPU is restricted by the video display.

The format of the display area under the control of the VDG is actually 256 'dots' across by 192 'dots' down giving a total of 49 152 fundamental picture elements (pixels) under the 'control' of the VDG. Each pixel may be one of up to eight colours, depending upon the mode selected (see Figure 1.).



* One on each non-interlaced line. For interlace, the lines of the odd field are copied into the even field thus doubling the number of displayed dots.

Figure 1. Typical Format of the Monitor Screen. The border is black in Alphanumeric and Semigraphic modes and green or buff in Graphic modes.

As you will have observed, the MC6847 does not utilise the entire video screen. The standard video screen consists of 262 scan lines extending across the screen, but the usable display window is offset from the top by 25 lines and extends 192 lines down the screen with a further 25 lines at the bottom being offset. Across the screen, the timing pulses are blanked-off to reduce the useable horizontal width. The linearity of images is better in the central portion of a screen and this is used by the VDG.

The screen is 'memory mapped' with each pixel on the screen being represented by a byte (or a number of bits thereof) in the video RAM. There is a one-to-one correspondence between the X-Y location of the pixel on the screen and the address of its control information in memory. The sequence of memory addresses, which are accessed to extract data to be converted to a video signal, is controlled by the VDG. The VDG also keeps track of the position of the moving spot and produces the necessary timing signals to synchronise the display to the computer. It produces, for instance, the horizon- ▶

tal sync pulse to indicate when the end of the video line has been reached so that the spot can 'flyback' to the beginning of the next scan line. This pulse also permits the MPU to access video memory during the blanking period, thereby avoiding flicker.

The decoding of the data input to the VDG is usually done by a character generator. This may be a pre-programmed, on-chip ROM in the MC6847 or an external, perhaps programmable, character generator.

The display modes that the MC6847 may operate in are set out in Table 1. this tabulation summarises much of the information about the VDG chip. The way in which these features are selected is in-line with most digital devices. The pin assignment diagram for the MC6847 is shown on Figure 2. The chip is an N-channel, silicon gate device with most signals being TTL compatible. The device is housed in a 40-pin DIL package. The amount of memory required by the various display modes is a trade-off against element size or resolution of the display in pixels. This feature will become more apparent later.

The lines into, or out of, the VDG can be grouped into six classes but classes i) to iv) are the most important to this discussion.

i) **Address Lines.** (DAO — DA12) These permit up to 8K of video memory to be directly addressed, although only 6K is ever required. The absolute location of the video memory in the computer system will depend upon the address decoding used. The starting address is located at the upper left-hand corner of the screen. The activity of the address lines is regulated by the *MS pin and the display mode selected.

ii) **Date Lines.** (DDO — DD7) These are used to input values in RAM memory to be mapped onto the screen. The values are decoded within the chip with repsect to shape, luminance and chroma (see later).

iii) **Mode control Lines.** There are eight important lines into the VDG which control the 14 display modes. These are detailed in Table 1. Three major types of display may be selected: **(a)** Alphanumerics, **(b)** Semigraphics and, **(c)** Graphics.

The implementation of these displays within the VDG is quite different in each case.

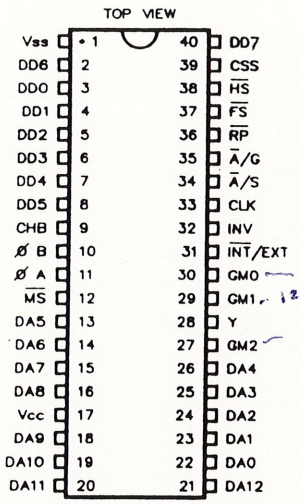


Figure 2. Pin-out for Motorola MC6847 Video Display Generator chip as used in the VZ computers.

Switching the screen to Alphanumerics or Graphics mode is determined by the (*A/G) line.

Switching the screen between Alphanumerics or Semigraphics mode is set by the (*A/S) line.

Selection of the internal (on-chip) or external character sets held in ROM is set by the (*INT/EXT) line. In Semigraphics mode this line determines whether SG4 or SG6 mode is selected.

Normal or inverse Alphanumeric displays are set by the (INV) line. Three lines (GMO, GM1, GM2) are used to select one-of-eight Graphics modes to be used.

An eighth control line (CSS) selects the colour set to be used in the particular mode selected. Most modes have two colour sets available.

In Alphanumeric and Semigraphics 4 modes, one-of-two background colours is selected and in Semigraphics 6 and Full Graphics modes one-of-two colour sets is selected.

The operating mode of *A/S, *INT/EXT, CSS and INV may be changed on a character by character basis in Alphanumerics and Semigraphics mode.

TABLE 1:
SUMMARY OF DISPLAY MODES FOR MC6847 VDG

	colours available	bytes video RAM	memory mapping	element size	Control Lines *A/G	*A/S	*INT/EXT	INV	GMO	GM1	GM2
Four ALPHANUMERIC Display Modes											
i) Internal ROM Alphanumerics	2	512	byte	BX12	0	0	0	0	x	x	x
ii) Internal ROM Alphanumerics — Inverted	2	512	byte	BX12	0	0	0	1	x	x	x
iii) External ROM Alphanumerics	2	512	byte	BX12	0	0	1	0	x	x	x
iv) External ROM Alphanumerics — Inverted	2	512	byte	BX12	0	0	1	1	x	x	x
Two SEMI-GRAPHIC Display Modes											
v) 32 by 16 Semigraphics 4 (SG4)	8	512	byte	BX12	0	1	0	x	x	x	x
vi) 32 By 16 Semigraphics 6 (SG6)	4	512	byte	BX12	0	1	1	x	x	x	x
Eight GRAPHIC Display Modes											
vii) 64 by 64 Colour Graphics One (CG1)	4	1024	2 bit	3x4	1	x	x	x	0	0	0
iix) 128 by 64 Resolution Graphics One (RG1)	2	1024	1 bit	2x3	1	x	x	x	0	0	1
ix) 128 by 64 Colour Graphics Two (CG2)	4	2048	2 bit	2x3	1	x	x	x	0	1	0
x) 128 by 96 Resolution Graphics Two (RG2)	2	1536	1 bit	2x2	1	x	x	x	0	1	1
xi) 128 by 96 Colour Graphics Three (CG3)	4	3072	2 bit	2x2	1	x	x	x	1	0	0
xii) 128 by 192 Resolution Graphics Three (RG3)	2	3072	1 bit	sx1	1	x	x	x	1	0	1
xiii) 128 by 192 Colour Graphics Six (CG6)	4	6144	2 bit	2x1	1	x	x	x	1	1	0
xiv) 256 by 192 Resolution Graphics Six (RG6)	2	6144	1 bit	1x1	1	x	x	x	1	1	1

The IEEE standard for electrical state relationships uses the suffix '' instead of the overbar '−' to designate when an electrical signal is active low.*

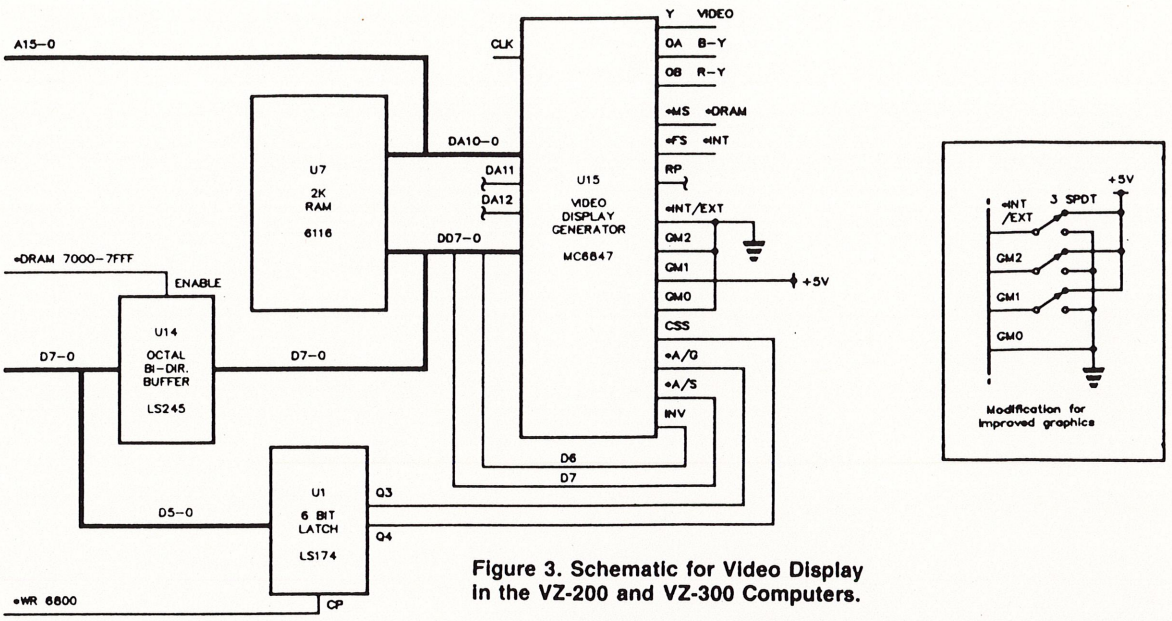


Figure 3. Schematic for Video Display in the VZ-200 and VZ-300 Computers.

iv) Power Supply.
Vss: 0 V supply — normally ground.
Vcc: +5 supply.

v) Video Lines.
These are four analogue signals:

OA B-Y chroma — a three-level signal used in combination with OB and Y to specify one-of-eight colours.

OB R-Y chroma — a four-level signal; the fourth is used as colour burst timing reference.

Y luminance — a six-level signal containing composite sync, blanking and four levels of luminance.

CHB chroma bias or a test point — not used in applications.

vi) Device Synchronising Controls.

*MS memory select, three-state control to allow the MPU to address the video RAM.

CLK 3.579 MHz clock.

*FS field sync to indicate the end of the active display area during which time the MPU may have access to the video RAM without causing undesirable flicker on the screen.

*HS horizontal sync to the TV receiver.

*RP row preset — important when an external character generator ROM is used.

From this brief description, a grasp of how the VDG operates may be gleaned. We will now examine how this particular VDG chip is used in a home computer application — the VZ computer.

The MC6847 in the VZ-200/300 computer

In the VZ computer a number of display modes using the MC6847 are available. Specifically, modes (i), (ii), (v) and (ix) on Table 1 are implemented as standard on the VZ. These modes are 'soft switched' or software selectable from the ROM-resident BASIC and will be described in detail later in this article.

The video display system in the VZ consists of a number of components or 'blocks' — but the heart of the display system is the VDG just described. This device interfaces with 2K of dynamic video RAM which occupies 7000H to 77FFH of the memory map for the Z80A MPU used in the VZs. Additionally, a hex write-only latch mapped at 6800H (but extending to 6FFFH due to simplified address decoding) controls, via software, the display modes implemented on the VZ.

The analogue outputs from the BDG are processed by further video circuitry which need not concern us here. All of these blocks are synchronised by a 3.58 MHz clock. This is an instance where the full speed of the Z80A (4 MHz) is not realised due to impositions by the video display.

More significantly however, the architecture of the VZ has only allowed 2K of RAM for the video display. This effectively prohibits the implementation of some of the hi-res graphics modes. [Specifically, modes (xi) to (xiv) in Table 1]. The VZ does not contain an external character generator ROM and relies entirely upon the VDG on-chip character ROM. Clearly, the VZ is manufactured to a price (and a very attractive one at that!) and was designed to interface with Microsoft's BASIC Level II ROM routines. Despite these comments, there are opportunities to make a few slight and simple changes to the hardware around the VDG to implement additional display modes with improved resolution. It is also possible to add an external character generator — but more of these later.

Figure 3 is a diagrammatic representation of the way in which the MC6847 VDG is interconnected in the VZ computers. The address lines DAO-DA10 (11 lines) are connected to U7 — a 6116 2K RAM chip — which is mapped as the video RAM section of memory. Lines DA11 and DA12 are not connected, thereby limiting the addressable video memory to 2K. Data lines DDO-DD7 (eight lines) are connected into the data bus from the MPU of which the 2K video RAM memory of course forms a part. The way in which the eight control lines are connected is of interest as these determine the type of displays available on the VZ.

Reference to Table 1 will indicate how the control lines are configured. The Graphics display group consist of GM0, GM1 and GM2. As can be seen from Figure 3, both GM0 and GM2 are tied low (to ground) whilst GM1 is tied high, to the +5 V Supply. Similarly, *INT/EXT is permanently tied low, thereby enabling the on-chip character generator ROM. The configuration of GM0-GM2 to 010B means that only Colour Graphics Two (CG2) is implemented when Graphics mode is selected. ▶

The remaining four control lines are interesting as they are not 'hard-wired' but are set up to be 'soft switched' — although two quite different techniques are used.

The INV line is connected to bit 6, or DD6, of the data bus. Thus, whilst in Alphanumeric mode, the second most significant bit of a byte contained in video RAM controls whether a normal or inverse character is displayed. The line that selects between Alphanumeric and Semigraphic modes — *A/S — is similarly connected to the most significant bit or DD7. thus this bit determines whether the VDG should interpret a particular byte as an ASCII character or a graphics shape.

The remaining two lines are connected into the Output Latch mapped into 6800H. As mentioned before, this is a 6-bit write-only latch. It permits certain software commands to set or reset a particular bit of the latch and hence switch or control specific hardware interfaces. Figure 4 is a schematic of the portions of the latch which is of interest to us here. A copy of the latch is held in RAM at location 783BH. The *A/G line, which selects between hi- or lo-res screens, is connected to bit 3 of the Output Latch. If this bit is low or 0, then the screen is in lo-res mode which corresponds to Alphanumeric and Semigraphic modes. If the bit is high or 1, then hi-res or Graphics (CG2) mode is selected. It is quite simple to see that the MODE (X) command in BASIC directly sets this bit of the latch — where X maybe 1 or 0. Note that bit 3 of the latch corresponds to a value of 0BH on the latch.

The Colour Select line (CSS) is connected to bit 4 on the latch which maps as a value of 0FH. The effect of this line differs according to the mode selected. The CSS pin selects the background colour of the display and in so doing determines the colour set which may be displayed. When CSS is low or 0 the background colour is green, but if set high or 1, then in lo-res the background colour is orange, but if in hi-res then the background is buff. Sounds a little confusing — but actually it isn't, given a little thought and reflection on Table 1 and Figure 1. Furthermore, in hi-res mode this pin selects which of the two colour sets (each containing four colours) will be selected. Colour set 0 consists of green, yellow, blue and red, whilst colour set 1 consists of buff, cyan, magenta and orange. Clearly, this pin is set by the COLOR F, B command where B determines the background colour and F determines foreground colour.

An understanding of the operation of the mode control lines gives a good insight into how the BASIC interpreter interfaces with the hardware and the real world via the screen display.

For the hardware enthusiasts, and others closely following this article, the penny should have dropped as to how other screen modes can be made selectable on the VZ by some simple hardware alterations.

Improved graphics on the VZ computer

One of the disappointing features of the graphics capability of the VZ is that the Semigraphics (SG4) and Graphics (CG2) modes have rectangular characters and elements which considerably detract from the appearance of the displays. This feature can be remedied.

The following simple hardware modifications are outlined for those who feel they are competent tackle it. They involve the installation of three switches on the VZ. Figure 3 provides an indication of what is required.

If *INT/EXT can be switched high, then Semigraphic mode SG6 becomes available on the computer. This has the advantage of giving higher screen resolution and, although the characters are still rectangular, their elements are square rather than rectangular as in the standard implementation of SG4 mode.

In Graphics mode, only CG2 is available in the VZ. By switching GM1 and GM2 it is possible with the 2K of video

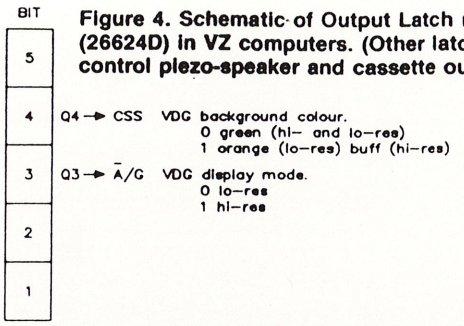


Figure 4. Schematic of Output Latch mapped at 6800H (26624D) in VZ computers. (Other latches are used to control piezo-speaker and cassette output)

memory to implement a further three modes (CG1, RG1 and RG2). There is little point in switching GM0 as there is insufficient memory to cover modes (xi) to (xiv). The element size in SG6 and CG1 is the same (3x4 pixels) and so there is little to choose between them — although their usage of memory is different and the characters in SG6 mode can be 'specified' through the keyboard as is done in SG4 mode on the VZ.

RG1 has the same resolution as the standard MODE (1) display but is only two-colour and consequently uses only half the memory space. the real benefit of adding the switches is in obtaining RG2 mode on the VZ. Although this only two colour, the element size is 2x2 pixels and is square. This is a great mode for plotting graphs for instance, where the screen resolution is 128 elements across by 96 elements down the screen.

To achieve this modification, use three SPDT toggle switches. Wire one side of each switch to +5 V, or pin 17 on the VDG, and wire the other side of each switch to ground or pin 1 of the chip. Cut the tracks leading from pins 27, 29 and 31 (GM2, GM1 and *INT/EXT) and wire the chip side to the centre terminal of a switch. This enables the three control lines to be switched high or low. (See inset on Figure 3.)

There you have it! It remains now to develop suitable software to drive these additional modes. The possibilities opened by the 'square' modes of SG6 and RG2 are exciting. (Who is going to submit some drivers for this conversion?)

As an afterthought, whilst you have got the VZ on the bench, why not add a RESET switch? A normally closed push-button switch inserted into the 'reset on power-up' line overcomes the annoying business of powering-down the VZ for resetting.

— continued next month.

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